---------- Begin Simulation Statistics ----------

sim\_seconds 0.000019 # Number of seconds simulated

sim\_ticks 18735000 # Number of ticks simulated

final\_tick 18735000 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)

sim\_freq 1000000000000 # Frequency of simulated ticks

host\_inst\_rate 85986 # Simulator instruction rate (inst/s)

host\_op\_rate 85967 # Simulator op (including micro ops) rate (op/s)

host\_tick\_rate 324852884 # Simulator tick rate (ticks/s)

host\_mem\_usage 642652 # Number of bytes of host memory used

host\_seconds 0.06 # Real time elapsed on the host

sim\_insts 4957 # Number of instructions simulated

sim\_ops 4957 # Number of ops (including micro ops) simulated

system.voltage\_domain.voltage 1 # Voltage in Volts

system.clk\_domain.clock 1000 # Clock period in ticks

system.mem\_ctrls.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.mem\_ctrls.bytes\_read::.cpu.inst 23104 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::.cpu.data 9280 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::total 32384 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::.cpu.inst 23104 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::total 23104 # Number of instructions bytes read from this memory

system.mem\_ctrls.num\_reads::.cpu.inst 361 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::.cpu.data 145 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::total 506 # Number of read requests responded to by this memory

system.mem\_ctrls.bw\_read::.cpu.inst 1233199893 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::.cpu.data 495329597 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::total 1728529490 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::.cpu.inst 1233199893 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::total 1233199893 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.inst 1233199893 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.data 495329597 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::total 1728529490 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.avgPriority\_.writebacks::samples 62.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.inst::samples 361.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.data::samples 145.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (s)

system.mem\_ctrls.priorityMaxLatency 0.000022840750 # per QoS priority maximum request to response latency (s)

system.mem\_ctrls.numReadWriteTurnArounds 2 # Number of turnarounds from READ to WRITE

system.mem\_ctrls.numWriteReadTurnArounds 2 # Number of turnarounds from WRITE to READ

system.mem\_ctrls.numStayReadState 1050 # Number of times bus staying in READ state

system.mem\_ctrls.numStayWriteState 30 # Number of times bus staying in WRITE state

system.mem\_ctrls.readReqs 506 # Number of read requests accepted

system.mem\_ctrls.writeReqs 62 # Number of write requests accepted

system.mem\_ctrls.readBursts 506 # Number of DRAM read bursts, including those serviced by the write queue

system.mem\_ctrls.writeBursts 62 # Number of DRAM write bursts, including those merged in the write queue

system.mem\_ctrls.bytesReadDRAM 32384 # Total number of bytes read from DRAM

system.mem\_ctrls.bytesReadWrQ 0 # Total number of bytes read from write queue

system.mem\_ctrls.bytesWritten 2048 # Total number of bytes written to DRAM

system.mem\_ctrls.bytesReadSys 32384 # Total read bytes from the system interface side

system.mem\_ctrls.bytesWrittenSys 3968 # Total written bytes from the system interface side

system.mem\_ctrls.servicedByWrQ 0 # Number of DRAM read bursts serviced by the write queue

system.mem\_ctrls.mergedWrBursts 0 # Number of DRAM write bursts merged with an existing one

system.mem\_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write

system.mem\_ctrls.perBankRdBursts::0 80 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::1 40 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::2 54 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::3 52 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::4 36 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::5 72 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::6 101 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::7 16 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::8 2 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::9 25 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::10 0 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::11 0 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::12 17 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::13 9 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::14 1 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::15 1 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::0 12 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::1 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::2 6 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::3 3 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::4 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::5 3 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::6 8 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::7 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::8 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::9 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::10 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::11 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::12 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::13 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::14 0 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::15 0 # Per bank write bursts

system.mem\_ctrls.numRdRetry 0 # Number of times read queue was full causing retry

system.mem\_ctrls.numWrRetry 0 # Number of times write queue was full causing retry

system.mem\_ctrls.totGap 18702000 # Total gap between requests

system.mem\_ctrls.readPktSize::0 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::1 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::2 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::3 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::4 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::5 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::6 506 # Read request sizes (log2)

system.mem\_ctrls.writePktSize::0 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::1 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::2 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::3 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::4 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::5 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::6 62 # Write request sizes (log2)

system.mem\_ctrls.rdQLenPdf::0 253 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::1 161 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::2 55 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::3 24 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::4 11 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::5 2 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::6 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::7 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::8 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::9 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::10 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::11 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::13 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::14 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::15 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::16 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::17 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::18 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::19 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::20 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::21 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::24 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::25 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::26 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::27 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::28 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::29 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::30 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::31 0 # What read queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::0 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::1 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::2 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::3 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::4 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::5 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::6 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::7 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::8 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::9 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::10 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::11 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::12 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::13 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::14 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::15 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::16 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::17 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::18 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::19 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::20 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::21 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::22 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::23 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::24 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::25 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::26 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::27 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::28 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::29 3 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::30 2 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::31 2 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::32 2 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::33 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::34 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::35 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::36 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::37 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::38 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::39 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::42 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::43 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::44 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::45 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::46 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::47 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::48 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::49 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::50 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::51 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::52 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::53 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::54 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::55 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::56 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::57 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::59 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::60 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::61 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::62 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::63 0 # What write queue length does an incoming req see

system.mem\_ctrls.bytesPerActivate::samples 91 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::mean 346.725275 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::gmean 207.947129 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::stdev 342.938351 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::0-127 28 30.77% 30.77% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::128-255 23 25.27% 56.04% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::256-383 9 9.89% 65.93% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::384-511 7 7.69% 73.63% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::512-639 3 3.30% 76.92% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::640-767 3 3.30% 80.22% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::768-895 2 2.20% 82.42% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::896-1023 6 6.59% 89.01% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::1024-1151 10 10.99% 100.00% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::total 91 # Bytes accessed per row activation

system.mem\_ctrls.rdPerTurnAround::samples 2 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::mean 233 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::gmean 127.530389 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::stdev 275.771645 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::32-47 1 50.00% 50.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::416-431 1 50.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::total 2 # Reads before turning the bus around for writes

system.mem\_ctrls.wrPerTurnAround::samples 2 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::mean 16 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::gmean 16.000000 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::16 2 100.00% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::total 2 # Writes before turning the bus around for reads

system.mem\_ctrls.masterReadBytes::.cpu.inst 23104 # Per-master bytes read from memory

system.mem\_ctrls.masterReadBytes::.cpu.data 9280 # Per-master bytes read from memory

system.mem\_ctrls.masterWriteBytes::.writebacks 2048 # Per-master bytes write to memory

system.mem\_ctrls.masterReadRate::.cpu.inst 1233199893.247931718826 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterReadRate::.cpu.data 495329597.010942101479 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterWriteRate::.writebacks 109314117.961035504937 # Per-master bytes write to memory rate (Bytes/sec)

system.mem\_ctrls.masterReadAccesses::.cpu.inst 361 # Per-master read serviced memory accesses

system.mem\_ctrls.masterReadAccesses::.cpu.data 145 # Per-master read serviced memory accesses

system.mem\_ctrls.masterWriteAccesses::.writebacks 62 # Per-master write serviced memory accesses

system.mem\_ctrls.masterReadTotalLat::.cpu.inst 11918500 # Per-master read total memory access latency

system.mem\_ctrls.masterReadTotalLat::.cpu.data 5201500 # Per-master read total memory access latency

system.mem\_ctrls.masterWriteTotalLat::.writebacks 157232000 # Per-master write total memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.inst 33015.24 # Per-master read average memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.data 35872.41 # Per-master read average memory access latency

system.mem\_ctrls.masterWriteAvgLat::.writebacks 2536000.00 # Per-master write average memory access latency

system.mem\_ctrls.totQLat 7632500 # Total ticks spent queuing

system.mem\_ctrls.totMemAccLat 17120000 # Total ticks spent from burst creation until serviced by the DRAM

system.mem\_ctrls.totBusLat 2530000 # Total ticks spent in databus transfers

system.mem\_ctrls.avgQLat 15083.99 # Average queueing delay per DRAM burst

system.mem\_ctrls.avgBusLat 5000.00 # Average bus latency per DRAM burst

system.mem\_ctrls.avgMemAccLat 33833.99 # Average memory access latency per DRAM burst

system.mem\_ctrls.avgRdBW 1728.53 # Average DRAM read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBW 109.31 # Average achieved write bandwidth in MiByte/s

system.mem\_ctrls.avgRdBWSys 1728.53 # Average system read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBWSys 211.80 # Average system write bandwidth in MiByte/s

system.mem\_ctrls.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s

system.mem\_ctrls.busUtil 14.36 # Data bus utilization in percentage

system.mem\_ctrls.busUtilRead 13.50 # Data bus utilization in percentage for reads

system.mem\_ctrls.busUtilWrite 0.85 # Data bus utilization in percentage for writes

system.mem\_ctrls.avgRdQLen 1.89 # Average read queue length when enqueuing

system.mem\_ctrls.avgWrQLen 13.10 # Average write queue length when enqueuing

system.mem\_ctrls.readRowHits 407 # Number of row buffer hits during reads

system.mem\_ctrls.writeRowHits 31 # Number of row buffer hits during writes

system.mem\_ctrls.readRowHitRate 80.43 # Row buffer hit rate for reads

system.mem\_ctrls.writeRowHitRate 50.00 # Row buffer hit rate for writes

system.mem\_ctrls.avgGap 32926.06 # Average gap between requests

system.mem\_ctrls.pageHitRate 77.11 # Row buffer hit rate, read and write combined

system.mem\_ctrls\_0.actEnergy 621180 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_0.preEnergy 303600 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_0.readEnergy 3220140 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_0.writeEnergy 167040 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_0.refreshEnergy 1229280.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_0.actBackEnergy 4573680 # Energy for active background per rank (pJ)

system.mem\_ctrls\_0.preBackEnergy 25920 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_0.actPowerDownEnergy 3938130 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_0.prePowerDownEnergy 480 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_0.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_0.totalEnergy 14079450 # Total energy per rank (pJ)

system.mem\_ctrls\_0.averagePower 751.505204 # Core power per rank (mW)

system.mem\_ctrls\_0.totalIdleTime 8631500 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_0.memoryStateTime::IDLE 12000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::REF 520000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::SREF 0 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::PRE\_PDN 1250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT 9563250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT\_PDN 8638500 # Time in different power states

system.mem\_ctrls\_1.actEnergy 92820 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_1.preEnergy 41745 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_1.readEnergy 392700 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_1.writeEnergy 0 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_1.refreshEnergy 1229280.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_1.actBackEnergy 892050 # Energy for active background per rank (pJ)

system.mem\_ctrls\_1.preBackEnergy 125280 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_1.actPowerDownEnergy 7065720 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_1.prePowerDownEnergy 367680 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_1.selfRefreshEnergy 0 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_1.totalEnergy 10207275 # Total energy per rank (pJ)

system.mem\_ctrls\_1.averagePower 544.823859 # Core power per rank (mW)

system.mem\_ctrls\_1.totalIdleTime 14630750 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_1.memoryStateTime::IDLE 272000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::REF 520000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::SREF 0 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::PRE\_PDN 956250 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT 1492250 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT\_PDN 15494500 # Time in different power states

system.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.cpu.branchPred.lookups 1993 # Number of BP lookups

system.cpu.branchPred.condPredicted 1260 # Number of conditional branches predicted

system.cpu.branchPred.condIncorrect 449 # Number of conditional branches incorrect

system.cpu.branchPred.BTBLookups 1581 # Number of BTB lookups

system.cpu.branchPred.BTBHits 555 # Number of BTB hits

system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.

system.cpu.branchPred.BTBHitPct 35.104364 # BTB Hit Percentage

system.cpu.branchPred.usedRAS 207 # Number of times the RAS was used to get a target.

system.cpu.branchPred.RASInCorrect 1 # Number of incorrect RAS predictions.

system.cpu.branchPred.indirectLookups 80 # Number of indirect predictor lookups.

system.cpu.branchPred.indirectHits 7 # Number of indirect target hits.

system.cpu.branchPred.indirectMisses 73 # Number of indirect misses.

system.cpu.branchPredindirectMispredicted 33 # Number of mispredicted indirect branches.

system.cpu\_voltage\_domain.voltage 1 # Voltage in Volts

system.cpu\_clk\_domain.clock 500 # Clock period in ticks

system.cpu.dtb.fetch\_hits 0 # ITB hits

system.cpu.dtb.fetch\_misses 0 # ITB misses

system.cpu.dtb.fetch\_acv 0 # ITB acv

system.cpu.dtb.fetch\_accesses 0 # ITB accesses

system.cpu.dtb.read\_hits 1335 # DTB read hits

system.cpu.dtb.read\_misses 29 # DTB read misses

system.cpu.dtb.read\_acv 0 # DTB read access violations

system.cpu.dtb.read\_accesses 1364 # DTB read accesses

system.cpu.dtb.write\_hits 971 # DTB write hits

system.cpu.dtb.write\_misses 16 # DTB write misses

system.cpu.dtb.write\_acv 0 # DTB write access violations

system.cpu.dtb.write\_accesses 987 # DTB write accesses

system.cpu.dtb.data\_hits 2306 # DTB hits

system.cpu.dtb.data\_misses 45 # DTB misses

system.cpu.dtb.data\_acv 0 # DTB access violations

system.cpu.dtb.data\_accesses 2351 # DTB accesses

system.cpu.itb.fetch\_hits 1641 # ITB hits

system.cpu.itb.fetch\_misses 219 # ITB misses

system.cpu.itb.fetch\_acv 0 # ITB acv

system.cpu.itb.fetch\_accesses 1860 # ITB accesses

system.cpu.itb.read\_hits 0 # DTB read hits

system.cpu.itb.read\_misses 0 # DTB read misses

system.cpu.itb.read\_acv 0 # DTB read access violations

system.cpu.itb.read\_accesses 0 # DTB read accesses

system.cpu.itb.write\_hits 0 # DTB write hits

system.cpu.itb.write\_misses 0 # DTB write misses

system.cpu.itb.write\_acv 0 # DTB write access violations

system.cpu.itb.write\_accesses 0 # DTB write accesses

system.cpu.itb.data\_hits 0 # DTB hits

system.cpu.itb.data\_misses 0 # DTB misses

system.cpu.itb.data\_acv 0 # DTB access violations

system.cpu.itb.data\_accesses 0 # DTB accesses

system.cpu.workload.numSyscalls 11 # Number of system calls

system.cpu.pwrStateResidencyTicks::ON 18735000 # Cumulative time (in ticks) in various power states

system.cpu.numCycles 37471 # number of cpu cycles simulated

system.cpu.numWorkItemsStarted 0 # number of work items this cpu started

system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed

system.cpu.fetch.icacheStallCycles 8693 # Number of cycles fetch is stalled on an Icache miss

system.cpu.fetch.Insts 10606 # Number of instructions fetch has processed

system.cpu.fetch.Branches 1993 # Number of branches that fetch encountered

system.cpu.fetch.predictedBranches 769 # Number of branches that fetch has predicted taken

system.cpu.fetch.Cycles 3321 # Number of cycles fetch has run and was not squashing or blocked

system.cpu.fetch.SquashCycles 1338 # Number of cycles fetch has spent squashing

system.cpu.fetch.MiscStallCycles 195 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs

system.cpu.fetch.PendingTrapStallCycles 1253 # Number of stall cycles due to pending traps

system.cpu.fetch.IcacheWaitRetryStallCycles 12 # Number of stall cycles due to full MSHR

system.cpu.fetch.CacheLines 1641 # Number of cache lines fetched

system.cpu.fetch.IcacheSquashes 353 # Number of outstanding Icache misses that were squashed

system.cpu.fetch.rateDist::samples 14143 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::mean 0.749912 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::stdev 2.086966 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::0 12157 85.96% 85.96% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::1 190 1.34% 87.30% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::2 225 1.59% 88.89% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::3 153 1.08% 89.97% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::4 177 1.25% 91.23% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::5 242 1.71% 92.94% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::6 154 1.09% 94.03% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::7 95 0.67% 94.70% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::8 750 5.30% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::min\_value 0 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::max\_value 8 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::total 14143 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.branchRate 0.053188 # Number of branch fetches per cycle

system.cpu.fetch.rate 0.283046 # Number of inst fetches per cycle

system.cpu.decode.IdleCycles 8654 # Number of cycles decode is idle

system.cpu.decode.BlockedCycles 3060 # Number of cycles decode is blocked

system.cpu.decode.RunCycles 1793 # Number of cycles decode is running

system.cpu.decode.UnblockCycles 137 # Number of cycles decode is unblocking

system.cpu.decode.SquashCycles 499 # Number of cycles decode is squashing

system.cpu.decode.BranchResolved 675 # Number of times decode resolved a branch

system.cpu.decode.BranchMispred 172 # Number of times decode detected a branch misprediction

system.cpu.decode.DecodedInsts 8926 # Number of instructions handled by decode

system.cpu.decode.SquashedInsts 589 # Number of squashed instructions handled by decode

system.cpu.rename.SquashCycles 499 # Number of cycles rename is squashing

system.cpu.rename.IdleCycles 8842 # Number of cycles rename is idle

system.cpu.rename.BlockCycles 423 # Number of cycles rename is blocking

system.cpu.rename.serializeStallCycles 1842 # count of cycles rename stalled for serializing inst

system.cpu.rename.RunCycles 1729 # Number of cycles rename is running

system.cpu.rename.UnblockCycles 808 # Number of cycles rename is unblocking

system.cpu.rename.RenamedInsts 8523 # Number of instructions processed by rename

system.cpu.rename.IQFullEvents 7 # Number of times rename has blocked due to IQ full

system.cpu.rename.LQFullEvents 155 # Number of times rename has blocked due to LQ full

system.cpu.rename.SQFullEvents 577 # Number of times rename has blocked due to SQ full

system.cpu.rename.RenamedOperands 5404 # Number of destination operands rename has renamed

system.cpu.rename.RenameLookups 10210 # Number of register rename lookups that rename has made

system.cpu.rename.int\_rename\_lookups 10165 # Number of integer rename lookups

system.cpu.rename.fp\_rename\_lookups 34 # Number of floating rename lookups

system.cpu.rename.CommittedMaps 3224 # Number of HB maps that are committed

system.cpu.rename.UndoneMaps 2180 # Number of HB maps that are undone due to squashing

system.cpu.rename.serializingInsts 74 # count of serializing insts renamed

system.cpu.rename.tempSerializingInsts 42 # count of temporary serializing insts renamed

system.cpu.rename.skidInsts 699 # count of insts added to the skid buffer

system.cpu.memDep0.insertedLoads 1471 # Number of loads inserted to the mem dependence unit.

system.cpu.memDep0.insertedStores 1114 # Number of stores inserted to the mem dependence unit.

system.cpu.memDep0.conflictingLoads 13 # Number of conflicting loads.

system.cpu.memDep0.conflictingStores 11 # Number of conflicting stores.

system.cpu.iq.iqInstsAdded 7711 # Number of instructions added to the IQ (excludes non-spec)

system.cpu.iq.iqNonSpecInstsAdded 53 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 7151 # Number of instructions issued

system.cpu.iq.iqSquashedInstsIssued 10 # Number of squashed instructions issued

system.cpu.iq.iqSquashedInstsExamined 2806 # Number of squashed instructions iterated over during squash; mainly for profiling

system.cpu.iq.iqSquashedOperandsExamined 1183 # Number of squashed operands that are examined and possibly removed from graph

system.cpu.iq.iqSquashedNonSpecRemoved 17 # Number of squashed non-spec instructions that were removed

system.cpu.iq.issued\_per\_cycle::samples 14143 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::mean 0.505621 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::stdev 1.187883 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::0 11053 78.15% 78.15% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::1 1293 9.14% 87.29% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::2 691 4.89% 92.18% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::3 443 3.13% 95.31% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::4 335 2.37% 97.68% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::5 216 1.53% 99.21% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::6 67 0.47% 99.68% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::7 35 0.25% 99.93% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::8 10 0.07% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::min\_value 0 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::max\_value 8 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::total 14143 # Number of insts issued each cycle

system.cpu.iq.fu\_full::No\_OpClass 0 0.00% 0.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntAlu 1 1.03% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntMult 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntDiv 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatAdd 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCmp 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCvt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMult 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMultAcc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatDiv 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMisc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatSqrt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAdd 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAddAcc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAlu 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCmp 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCvt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMisc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMult 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMultAcc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShift 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShiftAcc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSqrt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAdd 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAlu 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCmp 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCvt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatDiv 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMisc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMult 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMultAcc 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatSqrt 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAes 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAesMix 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha1Hash 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha1Hash2 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha256Hash 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha256Hash2 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShaSigma2 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShaSigma3 0 0.00% 1.03% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemRead 55 56.70% 57.73% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemWrite 38 39.18% 96.91% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemRead 0 0.00% 96.91% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemWrite 3 3.09% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.FU\_type\_0::No\_OpClass 199 2.78% 2.78% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntAlu 4489 62.77% 65.56% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntMult 4 0.06% 65.61% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntDiv 0 0.00% 65.61% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatAdd 12 0.17% 65.78% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCmp 0 0.00% 65.78% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCvt 10 0.14% 65.92% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMult 0 0.00% 65.92% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMultAcc 0 0.00% 65.92% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatDiv 2 0.03% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMisc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatSqrt 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAdd 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAddAcc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAlu 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCmp 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCvt 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMisc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMult 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMultAcc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShift 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShiftAcc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSqrt 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAdd 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAlu 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCmp 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCvt 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatDiv 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMisc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMult 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMultAcc 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatSqrt 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAes 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAesMix 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha1Hash 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha1Hash2 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha256Hash 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha256Hash2 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShaSigma2 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShaSigma3 0 0.00% 65.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemRead 1412 19.75% 85.69% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemWrite 999 13.97% 99.66% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemRead 6 0.08% 99.75% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemWrite 18 0.25% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::IprAccess 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::total 7151 # Type of FU issued

system.cpu.iq.rate 0.190841 # Inst issue rate

system.cpu.iq.fu\_busy\_cnt 97 # FU busy when requested

system.cpu.iq.fu\_busy\_rate 0.013565 # FU busy rate (busy events/executed inst)

system.cpu.iq.int\_inst\_queue\_reads 28453 # Number of integer instruction queue reads

system.cpu.iq.int\_inst\_queue\_writes 10529 # Number of integer instruction queue writes

system.cpu.iq.int\_inst\_queue\_wakeup\_accesses 6459 # Number of integer instruction queue wakeup accesses

system.cpu.iq.fp\_inst\_queue\_reads 99 # Number of floating instruction queue reads

system.cpu.iq.fp\_inst\_queue\_writes 51 # Number of floating instruction queue writes

system.cpu.iq.fp\_inst\_queue\_wakeup\_accesses 48 # Number of floating instruction queue wakeup accesses

system.cpu.iq.vec\_inst\_queue\_reads 0 # Number of vector instruction queue reads

system.cpu.iq.vec\_inst\_queue\_writes 0 # Number of vector instruction queue writes

system.cpu.iq.vec\_inst\_queue\_wakeup\_accesses 0 # Number of vector instruction queue wakeup accesses

system.cpu.iq.int\_alu\_accesses 6998 # Number of integer alu accesses

system.cpu.iq.fp\_alu\_accesses 51 # Number of floating point alu accesses

system.cpu.iq.vec\_alu\_accesses 0 # Number of vector alu accesses

system.cpu.iew.lsq.thread0.forwLoads 30 # Number of loads that had data forwarded from stores

system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address

system.cpu.iew.lsq.thread0.squashedLoads 541 # Number of loads squashed

system.cpu.iew.lsq.thread0.ignoredResponses 1 # Number of memory responses ignored because the instruction is squashed

system.cpu.iew.lsq.thread0.memOrderViolation 11 # Number of memory ordering violations

system.cpu.iew.lsq.thread0.squashedStores 241 # Number of stores squashed

system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address

system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding

system.cpu.iew.lsq.thread0.rescheduledLoads 1 # Number of loads that were rescheduled

system.cpu.iew.lsq.thread0.cacheBlocked 46 # Number of times an access to memory failed due to the cache being blocked

system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle

system.cpu.iew.iewSquashCycles 499 # Number of cycles IEW is squashing

system.cpu.iew.iewBlockCycles 255 # Number of cycles IEW is blocking

system.cpu.iew.iewUnblockCycles 175 # Number of cycles IEW is unblocking

system.cpu.iew.iewDispatchedInsts 8067 # Number of instructions dispatched to IQ

system.cpu.iew.iewDispSquashedInsts 58 # Number of squashed instructions skipped by dispatch

system.cpu.iew.iewDispLoadInsts 1471 # Number of dispatched load instructions

system.cpu.iew.iewDispStoreInsts 1114 # Number of dispatched store instructions

system.cpu.iew.iewDispNonSpecInsts 35 # Number of dispatched non-speculative instructions

system.cpu.iew.iewIQFullEvents 0 # Number of times the IQ has become full, causing a stall

system.cpu.iew.iewLSQFullEvents 175 # Number of times the LSQ has become full, causing a stall

system.cpu.iew.memOrderViolationEvents 11 # Number of memory order violations

system.cpu.iew.predictedTakenIncorrect 22 # Number of branches that were predicted taken incorrectly

system.cpu.iew.predictedNotTakenIncorrect 482 # Number of branches that were predicted not taken incorrectly

system.cpu.iew.branchMispredicts 504 # Number of branch mispredicts detected at execute

system.cpu.iew.iewExecutedInsts 6932 # Number of executed instructions

system.cpu.iew.iewExecLoadInsts 1364 # Number of load instructions executed

system.cpu.iew.iewExecSquashedInsts 219 # Number of squashed instructions skipped in execute

system.cpu.iew.exec\_swp 0 # number of swp insts executed

system.cpu.iew.exec\_nop 303 # number of nop insts executed

system.cpu.iew.exec\_refs 2351 # number of memory reference insts executed

system.cpu.iew.exec\_branches 1316 # Number of branches executed

system.cpu.iew.exec\_stores 987 # Number of stores executed

system.cpu.iew.exec\_rate 0.184996 # Inst execution rate

system.cpu.iew.wb\_sent 6769 # cumulative count of insts sent to commit

system.cpu.iew.wb\_count 6507 # cumulative count of insts written-back

system.cpu.iew.wb\_producers 2904 # num instructions producing a value

system.cpu.iew.wb\_consumers 3822 # num instructions consuming a value

system.cpu.iew.wb\_rate 0.173654 # insts written-back per cycle

system.cpu.iew.wb\_fanout 0.759812 # average fanout of values written-back

system.cpu.commit.commitSquashedInsts 2839 # The number of squashed insts skipped by commit

system.cpu.commit.commitNonSpecStalls 36 # The number of times commit has been forced to stall to communicate backwards

system.cpu.commit.branchMispredicts 461 # The number of times a branch was mispredicted

system.cpu.commit.committed\_per\_cycle::samples 13389 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::mean 0.385092 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::stdev 1.201485 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::0 11328 84.61% 84.61% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::1 995 7.43% 92.04% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::2 359 2.68% 94.72% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::3 198 1.48% 96.20% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::4 160 1.20% 97.39% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::5 137 1.02% 98.42% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::6 63 0.47% 98.89% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::7 46 0.34% 99.23% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::8 103 0.77% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::min\_value 0 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::max\_value 8 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::total 13389 # Number of insts commited each cycle

system.cpu.commit.committedInsts 5156 # Number of instructions committed

system.cpu.commit.committedOps 5156 # Number of ops (including micro ops) committed

system.cpu.commit.swp\_count 0 # Number of s/w prefetches committed

system.cpu.commit.refs 1803 # Number of memory references committed

system.cpu.commit.loads 930 # Number of loads committed

system.cpu.commit.membars 12 # Number of memory barriers committed

system.cpu.commit.branches 951 # Number of branches committed

system.cpu.commit.vec\_insts 0 # Number of committed Vector instructions.

system.cpu.commit.fp\_insts 45 # Number of committed floating point instructions.

system.cpu.commit.int\_insts 4836 # Number of committed integer instructions.

system.cpu.commit.function\_calls 105 # Number of function calls committed.

system.cpu.commit.op\_class\_0::No\_OpClass 206 4.00% 4.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntAlu 3109 60.30% 64.29% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntMult 3 0.06% 64.35% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntDiv 0 0.00% 64.35% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatAdd 12 0.23% 64.58% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCmp 0 0.00% 64.58% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCvt 8 0.16% 64.74% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMult 0 0.00% 64.74% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMultAcc 0 0.00% 64.74% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatDiv 2 0.04% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMisc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatSqrt 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAdd 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAddAcc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAlu 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCmp 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCvt 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMisc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMult 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMultAcc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShift 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShiftAcc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSqrt 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAdd 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAlu 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCmp 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCvt 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatDiv 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMisc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMult 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMultAcc 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatSqrt 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAes 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAesMix 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha1Hash 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha1Hash2 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha256Hash 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha256Hash2 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShaSigma2 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShaSigma3 0 0.00% 64.78% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemRead 936 18.15% 82.93% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemWrite 857 16.62% 99.55% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemRead 6 0.12% 99.67% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemWrite 17 0.33% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::total 5156 # Class of committed instruction

system.cpu.commit.bw\_lim\_events 103 # number cycles where commit BW limit reached

system.cpu.rob.rob\_reads 20891 # The number of ROB reads

system.cpu.rob.rob\_writes 16746 # The number of ROB writes

system.cpu.timesIdled 246 # Number of times that the entire CPU went into an idle state and unscheduled itself

system.cpu.idleCycles 23328 # Total number of cycles that the CPU has spent unscheduled due to idling

system.cpu.committedInsts 4957 # Number of Instructions Simulated

system.cpu.committedOps 4957 # Number of Ops (including micro ops) Simulated

system.cpu.cpi 7.559209 # CPI: Cycles Per Instruction

system.cpu.cpi\_total 7.559209 # CPI: Total CPI of All Threads

system.cpu.ipc 0.132289 # IPC: Instructions Per Cycle

system.cpu.ipc\_total 0.132289 # IPC: Total IPC of All Threads

system.cpu.int\_regfile\_reads 8620 # number of integer regfile reads

system.cpu.int\_regfile\_writes 4416 # number of integer regfile writes

system.cpu.fp\_regfile\_reads 34 # number of floating regfile reads

system.cpu.fp\_regfile\_writes 24 # number of floating regfile writes

system.cpu.misc\_regfile\_reads 37 # number of misc regfile reads

system.cpu.misc\_regfile\_writes 28 # number of misc regfile writes

system.cpu.dcache.tags.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.cpu.dcache.tags.tagsinuse 98.162559 # Cycle average of tags in use

system.cpu.dcache.tags.total\_refs 1807 # Total number of references to valid blocks.

system.cpu.dcache.tags.sampled\_refs 146 # Sample count of references to valid blocks.

system.cpu.dcache.tags.avg\_refs 12.376712 # Average number of references to valid blocks.

system.cpu.dcache.tags.warmup\_cycle 159000 # Cycle when the warmup percentage was hit.

system.cpu.dcache.tags.occ\_blocks::.cpu.data 98.162559 # Average occupied blocks per requestor

system.cpu.dcache.tags.occ\_percent::.cpu.data 0.095862 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_percent::total 0.095862 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_task\_id\_blocks::1024 146 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::0 36 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::1 110 # Occupied blocks per task id

system.cpu.dcache.tags.occ\_task\_id\_percent::1024 0.142578 # Percentage of cache occupancy per task id

system.cpu.dcache.tags.tag\_accesses 4440 # Number of tag accesses

system.cpu.dcache.tags.data\_accesses 4440 # Number of data accesses

system.cpu.dcache.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.cpu.dcache.ReadReq\_hits::.cpu.data 1142 # number of ReadReq hits

system.cpu.dcache.ReadReq\_hits::total 1142 # number of ReadReq hits

system.cpu.dcache.WriteReq\_hits::.cpu.data 495 # number of WriteReq hits

system.cpu.dcache.WriteReq\_hits::total 495 # number of WriteReq hits

system.cpu.dcache.LoadLockedReq\_hits::.cpu.data 12 # number of LoadLockedReq hits

system.cpu.dcache.LoadLockedReq\_hits::total 12 # number of LoadLockedReq hits

system.cpu.dcache.StoreCondReq\_hits::.cpu.data 12 # number of StoreCondReq hits

system.cpu.dcache.StoreCondReq\_hits::total 12 # number of StoreCondReq hits

system.cpu.dcache.demand\_hits::.cpu.data 1637 # number of demand (read+write) hits

system.cpu.dcache.demand\_hits::total 1637 # number of demand (read+write) hits

system.cpu.dcache.overall\_hits::.cpu.data 1637 # number of overall hits

system.cpu.dcache.overall\_hits::total 1637 # number of overall hits

system.cpu.dcache.ReadReq\_misses::.cpu.data 120 # number of ReadReq misses

system.cpu.dcache.ReadReq\_misses::total 120 # number of ReadReq misses

system.cpu.dcache.WriteReq\_misses::.cpu.data 366 # number of WriteReq misses

system.cpu.dcache.WriteReq\_misses::total 366 # number of WriteReq misses

system.cpu.dcache.demand\_misses::.cpu.data 486 # number of demand (read+write) misses

system.cpu.dcache.demand\_misses::total 486 # number of demand (read+write) misses

system.cpu.dcache.overall\_misses::.cpu.data 486 # number of overall misses

system.cpu.dcache.overall\_misses::total 486 # number of overall misses

system.cpu.dcache.ReadReq\_miss\_latency::.cpu.data 7872000 # number of ReadReq miss cycles

system.cpu.dcache.ReadReq\_miss\_latency::total 7872000 # number of ReadReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::.cpu.data 18101485 # number of WriteReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::total 18101485 # number of WriteReq miss cycles

system.cpu.dcache.demand\_miss\_latency::.cpu.data 25973485 # number of demand (read+write) miss cycles

system.cpu.dcache.demand\_miss\_latency::total 25973485 # number of demand (read+write) miss cycles

system.cpu.dcache.overall\_miss\_latency::.cpu.data 25973485 # number of overall miss cycles

system.cpu.dcache.overall\_miss\_latency::total 25973485 # number of overall miss cycles

system.cpu.dcache.ReadReq\_accesses::.cpu.data 1262 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.ReadReq\_accesses::total 1262 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::.cpu.data 861 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::total 861 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::.cpu.data 12 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::total 12 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::.cpu.data 12 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::total 12 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.demand\_accesses::.cpu.data 2123 # number of demand (read+write) accesses

system.cpu.dcache.demand\_accesses::total 2123 # number of demand (read+write) accesses

system.cpu.dcache.overall\_accesses::.cpu.data 2123 # number of overall (read+write) accesses

system.cpu.dcache.overall\_accesses::total 2123 # number of overall (read+write) accesses

system.cpu.dcache.ReadReq\_miss\_rate::.cpu.data 0.095087 # miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_miss\_rate::total 0.095087 # miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::.cpu.data 0.425087 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::total 0.425087 # miss rate for WriteReq accesses

system.cpu.dcache.demand\_miss\_rate::.cpu.data 0.228921 # miss rate for demand accesses

system.cpu.dcache.demand\_miss\_rate::total 0.228921 # miss rate for demand accesses

system.cpu.dcache.overall\_miss\_rate::.cpu.data 0.228921 # miss rate for overall accesses

system.cpu.dcache.overall\_miss\_rate::total 0.228921 # miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_miss\_latency::.cpu.data 65600 # average ReadReq miss latency

system.cpu.dcache.ReadReq\_avg\_miss\_latency::total 65600 # average ReadReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::.cpu.data 49457.609290 # average WriteReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::total 49457.609290 # average WriteReq miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::.cpu.data 53443.384774 # average overall miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::total 53443.384774 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::.cpu.data 53443.384774 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::total 53443.384774 # average overall miss latency

system.cpu.dcache.blocked\_cycles::no\_mshrs 1505 # number of cycles access was blocked

system.cpu.dcache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_mshrs 29 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_mshrs 51.896552 # average number of cycles each access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.dcache.ReadReq\_mshr\_hits::.cpu.data 48 # number of ReadReq MSHR hits

system.cpu.dcache.ReadReq\_mshr\_hits::total 48 # number of ReadReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::.cpu.data 291 # number of WriteReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::total 291 # number of WriteReq MSHR hits

system.cpu.dcache.demand\_mshr\_hits::.cpu.data 339 # number of demand (read+write) MSHR hits

system.cpu.dcache.demand\_mshr\_hits::total 339 # number of demand (read+write) MSHR hits

system.cpu.dcache.overall\_mshr\_hits::.cpu.data 339 # number of overall MSHR hits

system.cpu.dcache.overall\_mshr\_hits::total 339 # number of overall MSHR hits

system.cpu.dcache.ReadReq\_mshr\_misses::.cpu.data 72 # number of ReadReq MSHR misses

system.cpu.dcache.ReadReq\_mshr\_misses::total 72 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::.cpu.data 75 # number of WriteReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::total 75 # number of WriteReq MSHR misses

system.cpu.dcache.demand\_mshr\_misses::.cpu.data 147 # number of demand (read+write) MSHR misses

system.cpu.dcache.demand\_mshr\_misses::total 147 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall\_mshr\_misses::.cpu.data 147 # number of overall MSHR misses

system.cpu.dcache.overall\_mshr\_misses::total 147 # number of overall MSHR misses

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::.cpu.data 5094000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::total 5094000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::.cpu.data 4702000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::total 4702000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::.cpu.data 9796000 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::total 9796000 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::.cpu.data 9796000 # number of overall MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::total 9796000 # number of overall MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::.cpu.data 0.057052 # mshr miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::total 0.057052 # mshr miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::.cpu.data 0.087108 # mshr miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::total 0.087108 # mshr miss rate for WriteReq accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::.cpu.data 0.069242 # mshr miss rate for demand accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::total 0.069242 # mshr miss rate for demand accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::.cpu.data 0.069242 # mshr miss rate for overall accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::total 0.069242 # mshr miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.data 70750 # average ReadReq mshr miss latency

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::total 70750 # average ReadReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::.cpu.data 62693.333333 # average WriteReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::total 62693.333333 # average WriteReq mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::.cpu.data 66639.455782 # average overall mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::total 66639.455782 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::.cpu.data 66639.455782 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::total 66639.455782 # average overall mshr miss latency

system.cpu.dcache.replacements 0 # number of replacements

system.cpu.icache.tags.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.cpu.icache.tags.tagsinuse 159.349781 # Cycle average of tags in use

system.cpu.icache.tags.total\_refs 1475 # Total number of references to valid blocks.

system.cpu.icache.tags.sampled\_refs 360 # Sample count of references to valid blocks.

system.cpu.icache.tags.avg\_refs 4.097222 # Average number of references to valid blocks.

system.cpu.icache.tags.warmup\_cycle 77000 # Cycle when the warmup percentage was hit.

system.cpu.icache.tags.occ\_blocks::.cpu.inst 159.349781 # Average occupied blocks per requestor

system.cpu.icache.tags.occ\_percent::.cpu.inst 0.311230 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_percent::total 0.311230 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_task\_id\_blocks::1024 298 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::0 192 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::1 106 # Occupied blocks per task id

system.cpu.icache.tags.occ\_task\_id\_percent::1024 0.582031 # Percentage of cache occupancy per task id

system.cpu.icache.tags.tag\_accesses 3642 # Number of tag accesses

system.cpu.icache.tags.data\_accesses 3642 # Number of data accesses

system.cpu.icache.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.cpu.icache.ReadReq\_hits::.cpu.inst 1115 # number of ReadReq hits

system.cpu.icache.ReadReq\_hits::total 1115 # number of ReadReq hits

system.cpu.icache.demand\_hits::.cpu.inst 1115 # number of demand (read+write) hits

system.cpu.icache.demand\_hits::total 1115 # number of demand (read+write) hits

system.cpu.icache.overall\_hits::.cpu.inst 1115 # number of overall hits

system.cpu.icache.overall\_hits::total 1115 # number of overall hits

system.cpu.icache.ReadReq\_misses::.cpu.inst 526 # number of ReadReq misses

system.cpu.icache.ReadReq\_misses::total 526 # number of ReadReq misses

system.cpu.icache.demand\_misses::.cpu.inst 526 # number of demand (read+write) misses

system.cpu.icache.demand\_misses::total 526 # number of demand (read+write) misses

system.cpu.icache.overall\_misses::.cpu.inst 526 # number of overall misses

system.cpu.icache.overall\_misses::total 526 # number of overall misses

system.cpu.icache.ReadReq\_miss\_latency::.cpu.inst 32171500 # number of ReadReq miss cycles

system.cpu.icache.ReadReq\_miss\_latency::total 32171500 # number of ReadReq miss cycles

system.cpu.icache.demand\_miss\_latency::.cpu.inst 32171500 # number of demand (read+write) miss cycles

system.cpu.icache.demand\_miss\_latency::total 32171500 # number of demand (read+write) miss cycles

system.cpu.icache.overall\_miss\_latency::.cpu.inst 32171500 # number of overall miss cycles

system.cpu.icache.overall\_miss\_latency::total 32171500 # number of overall miss cycles

system.cpu.icache.ReadReq\_accesses::.cpu.inst 1641 # number of ReadReq accesses(hits+misses)

system.cpu.icache.ReadReq\_accesses::total 1641 # number of ReadReq accesses(hits+misses)

system.cpu.icache.demand\_accesses::.cpu.inst 1641 # number of demand (read+write) accesses

system.cpu.icache.demand\_accesses::total 1641 # number of demand (read+write) accesses

system.cpu.icache.overall\_accesses::.cpu.inst 1641 # number of overall (read+write) accesses

system.cpu.icache.overall\_accesses::total 1641 # number of overall (read+write) accesses

system.cpu.icache.ReadReq\_miss\_rate::.cpu.inst 0.320536 # miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_miss\_rate::total 0.320536 # miss rate for ReadReq accesses

system.cpu.icache.demand\_miss\_rate::.cpu.inst 0.320536 # miss rate for demand accesses

system.cpu.icache.demand\_miss\_rate::total 0.320536 # miss rate for demand accesses

system.cpu.icache.overall\_miss\_rate::.cpu.inst 0.320536 # miss rate for overall accesses

system.cpu.icache.overall\_miss\_rate::total 0.320536 # miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_miss\_latency::.cpu.inst 61162.547529 # average ReadReq miss latency

system.cpu.icache.ReadReq\_avg\_miss\_latency::total 61162.547529 # average ReadReq miss latency

system.cpu.icache.demand\_avg\_miss\_latency::.cpu.inst 61162.547529 # average overall miss latency

system.cpu.icache.demand\_avg\_miss\_latency::total 61162.547529 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::.cpu.inst 61162.547529 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::total 61162.547529 # average overall miss latency

system.cpu.icache.blocked\_cycles::no\_mshrs 187 # number of cycles access was blocked

system.cpu.icache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_mshrs 4 # number of cycles access was blocked

system.cpu.icache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_mshrs 46.750000 # average number of cycles each access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.icache.writebacks::.writebacks 62 # number of writebacks

system.cpu.icache.writebacks::total 62 # number of writebacks

system.cpu.icache.ReadReq\_mshr\_hits::.cpu.inst 165 # number of ReadReq MSHR hits

system.cpu.icache.ReadReq\_mshr\_hits::total 165 # number of ReadReq MSHR hits

system.cpu.icache.demand\_mshr\_hits::.cpu.inst 165 # number of demand (read+write) MSHR hits

system.cpu.icache.demand\_mshr\_hits::total 165 # number of demand (read+write) MSHR hits

system.cpu.icache.overall\_mshr\_hits::.cpu.inst 165 # number of overall MSHR hits

system.cpu.icache.overall\_mshr\_hits::total 165 # number of overall MSHR hits

system.cpu.icache.ReadReq\_mshr\_misses::.cpu.inst 361 # number of ReadReq MSHR misses

system.cpu.icache.ReadReq\_mshr\_misses::total 361 # number of ReadReq MSHR misses

system.cpu.icache.demand\_mshr\_misses::.cpu.inst 361 # number of demand (read+write) MSHR misses

system.cpu.icache.demand\_mshr\_misses::total 361 # number of demand (read+write) MSHR misses

system.cpu.icache.overall\_mshr\_misses::.cpu.inst 361 # number of overall MSHR misses

system.cpu.icache.overall\_mshr\_misses::total 361 # number of overall MSHR misses

system.cpu.icache.ReadReq\_mshr\_miss\_latency::.cpu.inst 23383000 # number of ReadReq MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_latency::total 23383000 # number of ReadReq MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::.cpu.inst 23383000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::total 23383000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::.cpu.inst 23383000 # number of overall MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::total 23383000 # number of overall MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_rate::.cpu.inst 0.219988 # mshr miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_mshr\_miss\_rate::total 0.219988 # mshr miss rate for ReadReq accesses

system.cpu.icache.demand\_mshr\_miss\_rate::.cpu.inst 0.219988 # mshr miss rate for demand accesses

system.cpu.icache.demand\_mshr\_miss\_rate::total 0.219988 # mshr miss rate for demand accesses

system.cpu.icache.overall\_mshr\_miss\_rate::.cpu.inst 0.219988 # mshr miss rate for overall accesses

system.cpu.icache.overall\_mshr\_miss\_rate::total 0.219988 # mshr miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.inst 64772.853186 # average ReadReq mshr miss latency

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::total 64772.853186 # average ReadReq mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::.cpu.inst 64772.853186 # average overall mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::total 64772.853186 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::.cpu.inst 64772.853186 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::total 64772.853186 # average overall mshr miss latency

system.cpu.icache.replacements 62 # number of replacements

system.membus.snoop\_filter.tot\_requests 570 # Total number of requests made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_requests 63 # Number of requests hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_requests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.snoop\_filter.tot\_snoops 0 # Total number of snoops made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_snoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_snoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.pwrStateResidencyTicks::UNDEFINED 18735000 # Cumulative time (in ticks) in various power states

system.membus.trans\_dist::ReadResp 431 # Transaction distribution

system.membus.trans\_dist::WritebackClean 62 # Transaction distribution

system.membus.trans\_dist::ReadExReq 73 # Transaction distribution

system.membus.trans\_dist::ReadExResp 73 # Transaction distribution

system.membus.trans\_dist::ReadCleanReq 361 # Transaction distribution

system.membus.trans\_dist::ReadSharedReq 72 # Transaction distribution

system.membus.trans\_dist::InvalidateReq 2 # Transaction distribution

system.membus.pkt\_count\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 783 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 291 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count::total 1074 # Packet count per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 27008 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 9216 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size::total 36224 # Cumulative packet size per connected master and slave (bytes)

system.membus.snoops 0 # Total snoops (count)

system.membus.snoopTraffic 0 # Total snoop traffic (bytes)

system.membus.snoop\_fanout::samples 508 # Request fanout histogram

system.membus.snoop\_fanout::mean 0.001969 # Request fanout histogram

system.membus.snoop\_fanout::stdev 0.044368 # Request fanout histogram

system.membus.snoop\_fanout::underflows 0 0.00% 0.00% # Request fanout histogram

system.membus.snoop\_fanout::0 507 99.80% 99.80% # Request fanout histogram

system.membus.snoop\_fanout::1 1 0.20% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::2 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::overflows 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::min\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::max\_value 1 # Request fanout histogram

system.membus.snoop\_fanout::total 508 # Request fanout histogram

system.membus.reqLayer0.occupancy 924000 # Layer occupancy (ticks)

system.membus.reqLayer0.utilization 4.9 # Layer utilization (%)

system.membus.respLayer1.occupancy 1900000 # Layer occupancy (ticks)

system.membus.respLayer1.utilization 10.1 # Layer utilization (%)

system.membus.respLayer2.occupancy 767000 # Layer occupancy (ticks)

system.membus.respLayer2.utilization 4.1 # Layer utilization (%)

---------- End Simulation Statistics ----------